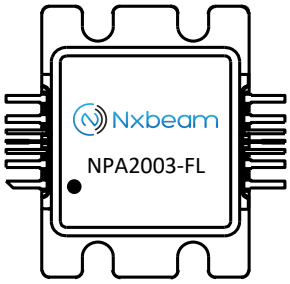
NPA2003-FL

27 – 31 GHz GaN 25 W Power Amplifier

Product Description

The Nxbeam NPA2003-FL is a GaN Ka-band high power amplifier in a high-performance leaded flange package. The part operates from 27 to 31 GHz and provides an average of 25 W saturated output power, 25% PAE, and 23 dB of linear gain. The part provide 15 W of linear power based on -30dBc spectral regrowth for a QPSK modulated signal. The amplifier consists of three gain stages that can be biased independently providing flexibility to tailor performance to specific application needs. The NPA2003-FL has RF input and output matched to 50 Ω with internal blocking capacitors for easy system integration.



Applications

- Ka-band Satellite Communications
- 5G Infrastructure
- Point-to-Point/Multipoint Digital Radios

Key Features

- Frequency: 27 – 31 GHz
- Linear Gain: 23 dB
- Psat (Ave.): 25 W
- PAE (Ave.): 25%
- Linear Power: 15 W (-30dBc SRG, QPSK, 10 MSPS)

Electrical Specifications

Test Condition: Vd = 24 V, Idq = 2.0 A, All Data is CW, Typical Performance at 25°C

Parameter		Min	Typical	Max	Unit
Frequency		27		31	GHz
Gain (Small Signal)	27 GHz		22		dB
	29 GHz		23		
	31 GHz		22		
Output Power (at Psat, Pin=26 dBm)	27 GHz		44		dBm
	29 GHz		44		
	31 GHz		44		
PAE (at Psat, Pin=26 dBm)	27 GHz		22		%
	29 GHz		25		
	31 GHz		25		
Power Gain (at Psat, Pin=26 dBm)	27 GHz		18		dB
	29 GHz		18		
	31 GHz		18		
Input Return Loss	27 GHz		17		dB
	29 GHz		17		
	31 GHz		18		
Output Return Loss	27 GHz		11		dB
	29 GHz		10		
	31 GHz		9		

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Absolute Maximum Ratings (Temp. = 25°C)

Parameter	Min	Max	Unit
Drain Voltage (Vd)		28	V
Drain Current (Id1)		660	mA
Drain Current (Id2)		1600	mA
Drain Current (Id3)		5250	mA
Gate Voltage (Vg1, Vg2, Vg3)	-8	0	V
Input Power (Pin)		TBD	dBm

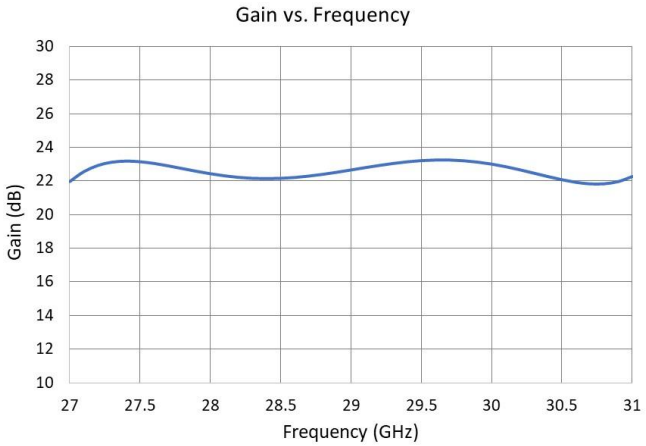
Recommended Operating Condition

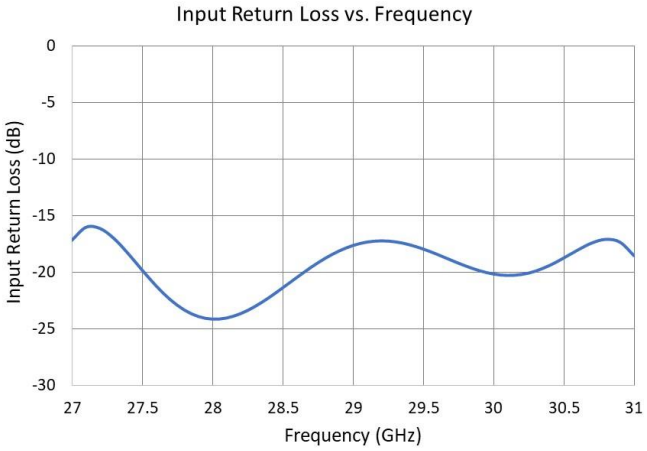
Parameter	Value	Unit
Drain Voltage (Vd)	20 - 28	V
Drain Current (Idq)	up to 3.2	A
Gate Voltage (Vg1, Vg2,Vg3) (Typical)	-4.0	V

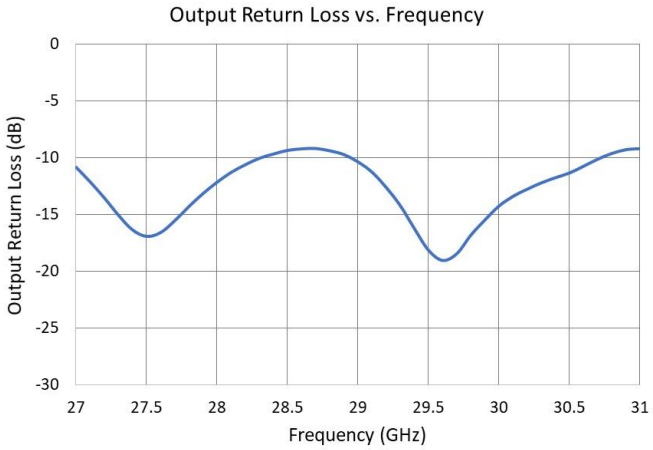
Small Signal Performance

Test Condition: Vd = 24 V, Idq = 2.0 A

(CW Performance at 25°C)







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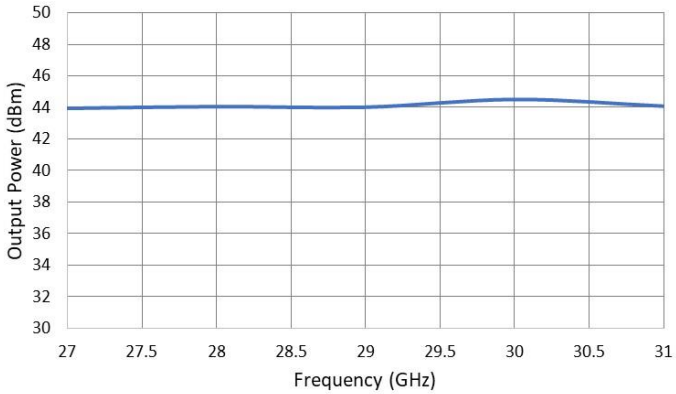
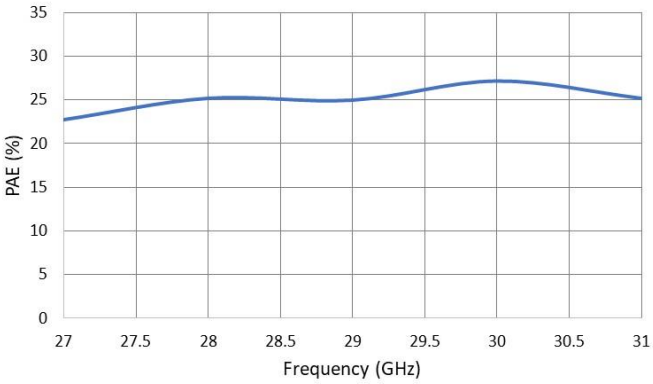
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 2.0 A, Pin = 26 dBm (Psat)
(CW Performance at 25°C)

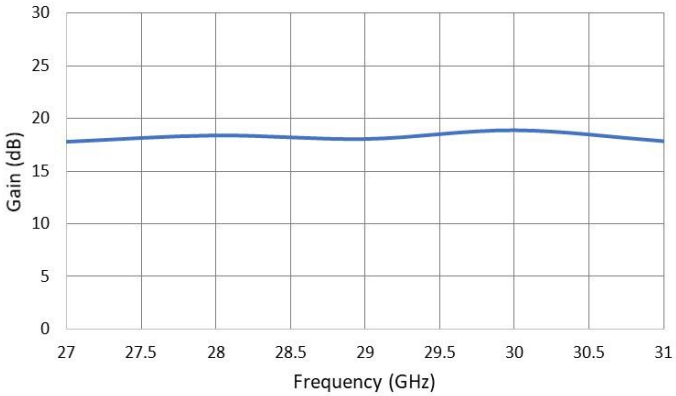
Output Power vs. Frequency (at 26 dBm Pin)



PAE vs. Frequency (at 26 dBm Pin)



Gain vs. Frequency (at 26 dBm Pin)



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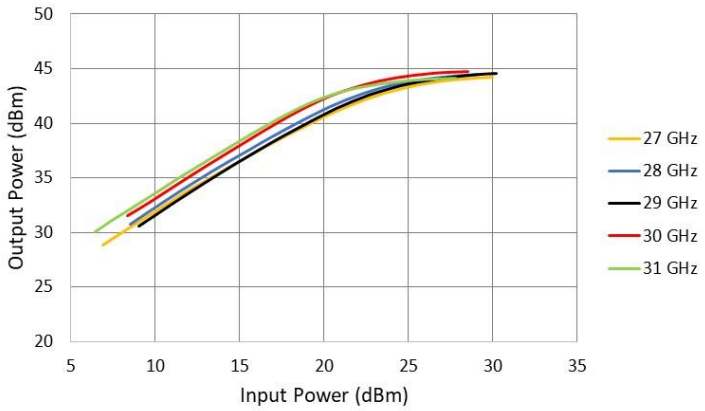
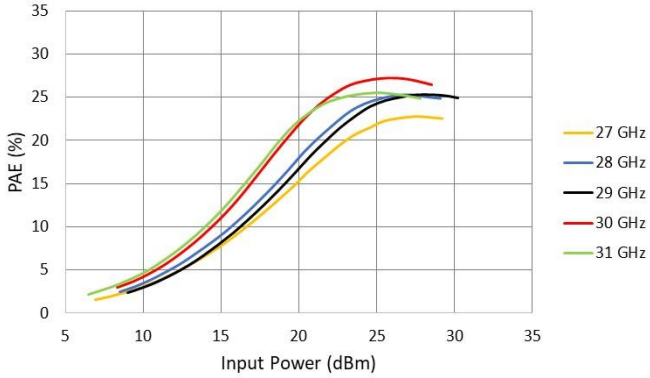
Large Signal Performance

Test Condition: Vd = 24 V, Idq = 2.0 A
(CW Performance at 25°C)

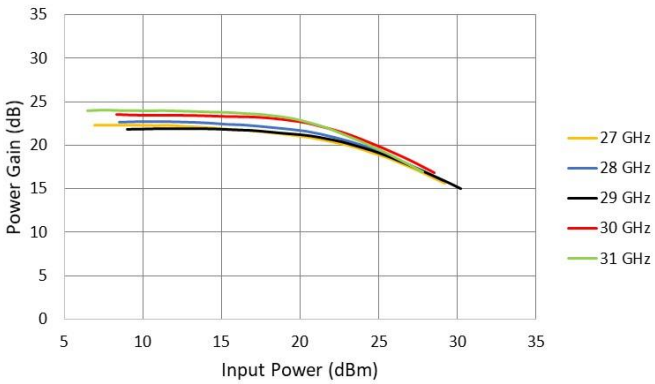
Output Power vs. Input Power vs. Frequency



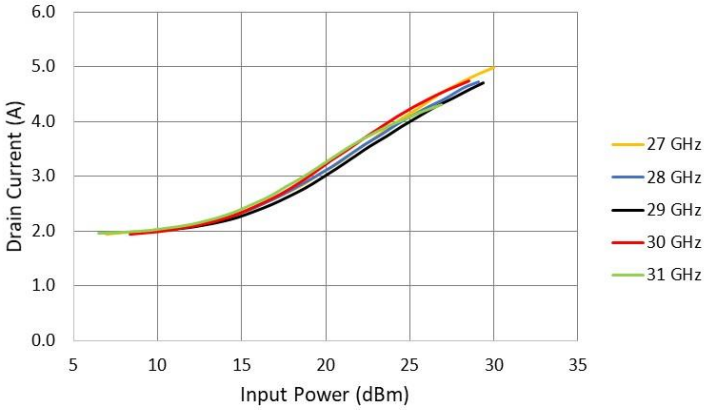
PAE vs. Input Power vs. Frequency



Power Gain vs. Input Power vs. Frequency



Drain Current vs. Input Power vs. Frequency



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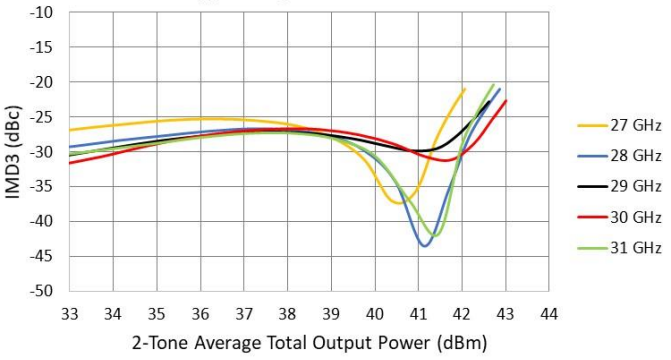
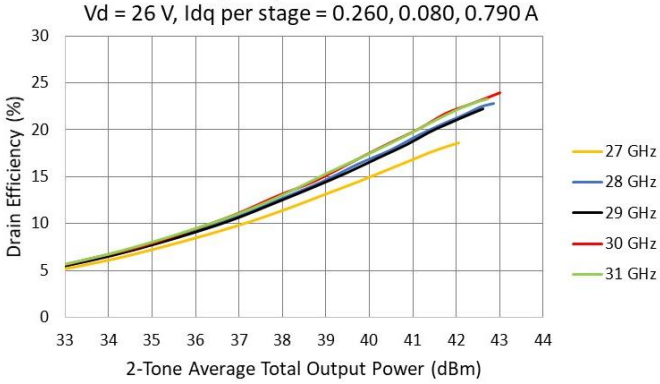
2-Tone Linearity Performance

Bias as Indicated in Figures, CW Performance at 25°C

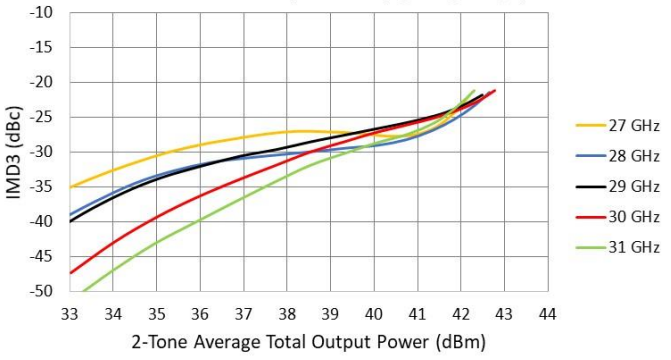
IMD3 vs. 2-Tone Output Power vs. Frequency
Frequency Offset= 10 MHz
Vd= 26 V, Idq per stage= 0.260, 0.080, 0.790 A



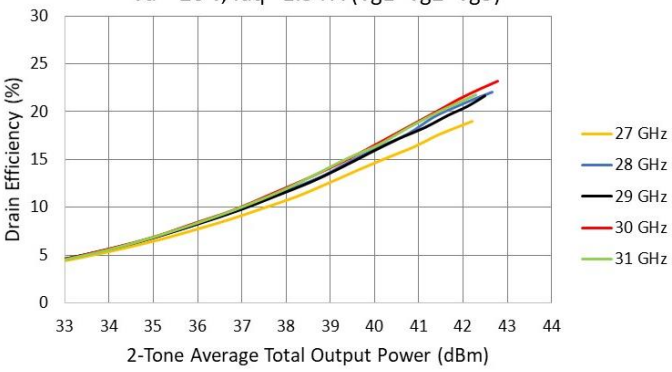
Drain Efficiency vs. 2-Tone Output Power vs. Frequency
Frequency Offset= 10 MHz
Vd = 26 V, Idq per stage = 0.260, 0.080, 0.790 A



IMD3 vs. 2-Tone Output Power vs. Frequency
Frequency Offset= 10 MHz
Vd= 26 V, Idq= 1.54 A (Vg1=Vg2=Vg3)



Drain Efficiency vs. 2-Tone Output Power vs. Frequency
Frequency Offset= 10 MHz
Vd = 26 V, Idq= 1.54 A (Vg1=Vg2=Vg3)



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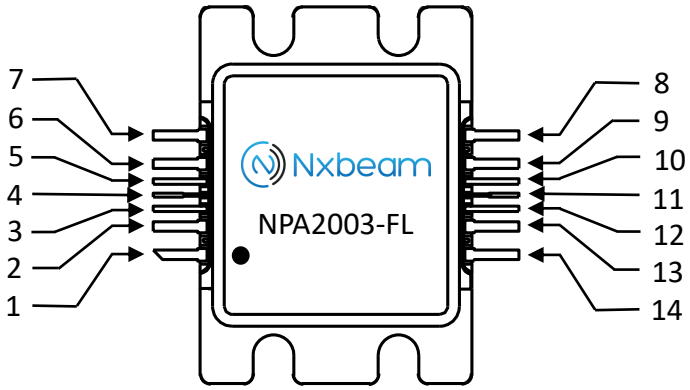
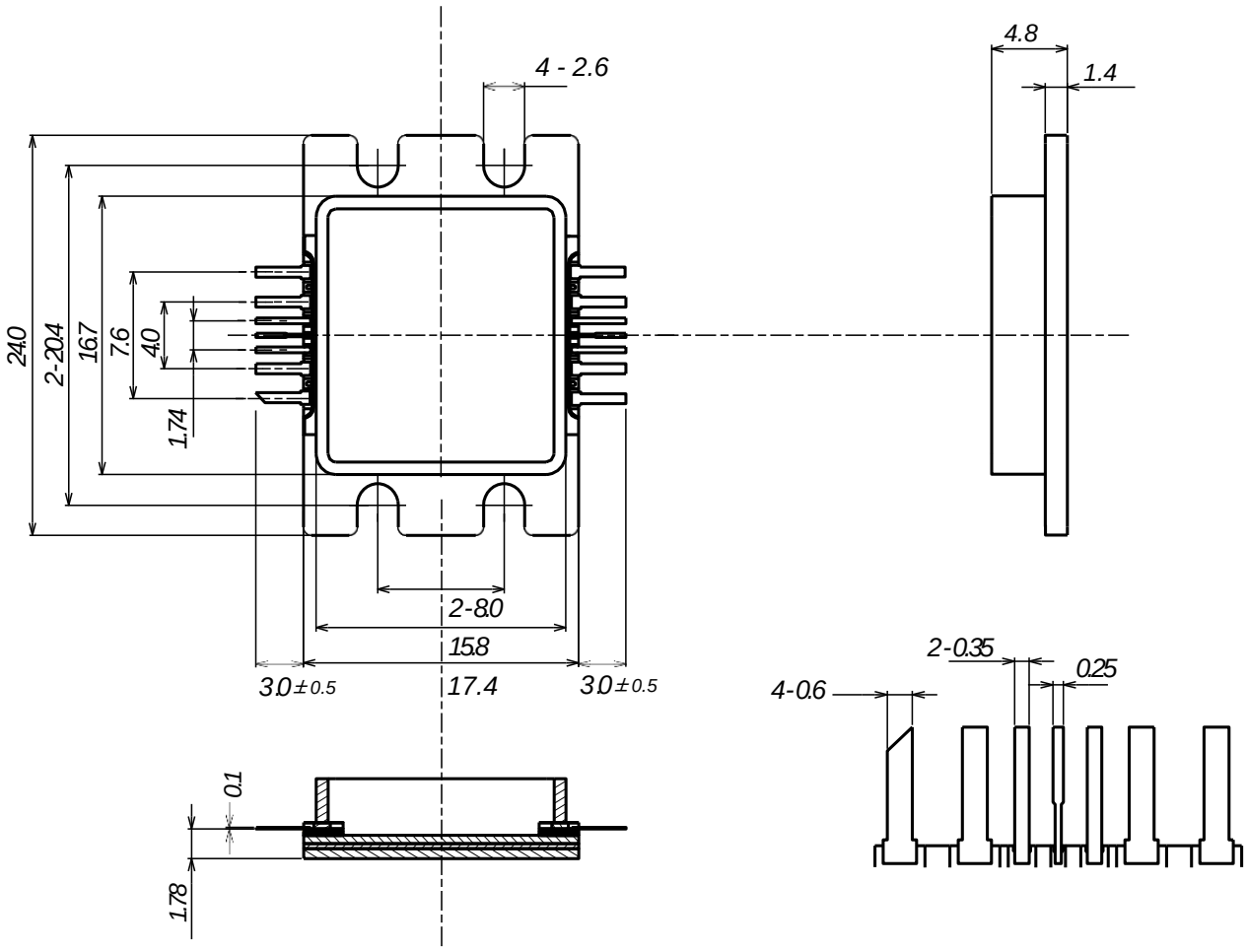
Package Pin Connection Information



Pad Num.	Function
1, 7	Vg2
2, 6	Vg1
3, 5, 10, 12	Gnd
4	RF in
8, 14	Vg3
9, 13	Vd
11	RF out

Package Dimensions (all dimensions in mm)



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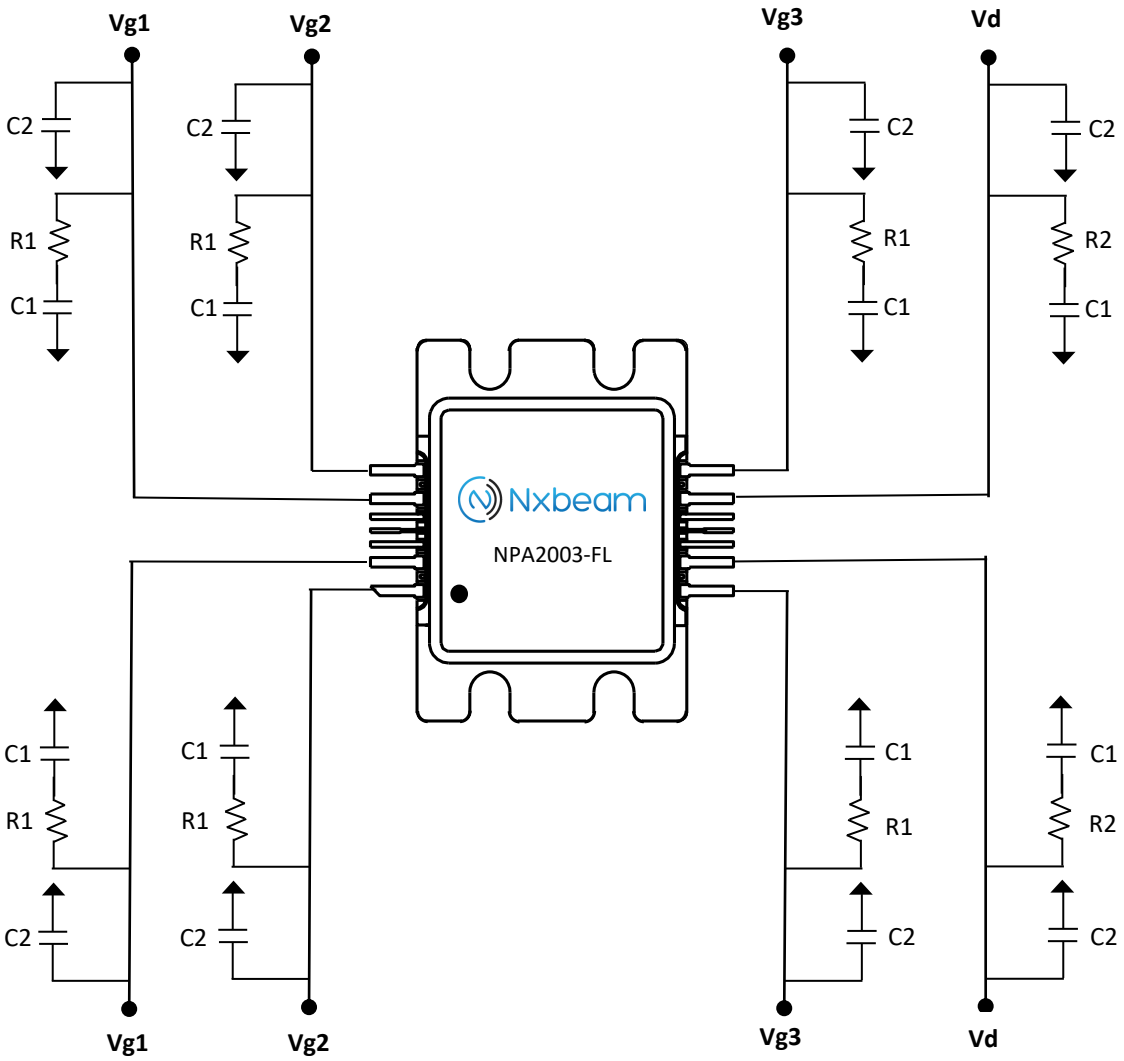
Suggested Off-Package Components

The following diagram shows the recommended off-package component.



Capacitor	Value
C1	0.1 µF
C2	10 µF

Resistor	Value
R1	10 Ω
R2	1 Ω

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Bias Information

Bias-up Procedure:
1.) It is recommended that voltage and current limits are set on the voltage supply's prior to biasing the product.
2.) Ensure power supplies are properly grounded to the product test fixture.
3.) Apply a negative voltage of -6 V to Vg1, Vg2, and Vg3 to ensure all devices are pinched off.
4.) Gradually increase the drain voltage, Vd, to the desired level but not to exceed the maximum voltage of 28 V.
5.) Gradually increase the gate voltages (Vg1, Vg2, Vg3) while monitoring the drain current until the desired drain current is achieved for each amplifier stage.
6.) Apply RF signal.

Bias-down Procedure:
1.) Turn off RF signal.
2.) Gradually decrease the gate voltages Vg1, Vg2, and Vg3 down to -6 V.
3.) Gradually decrease the drain voltage, Vd, down to 0 V.
4.) Gradually increase gate voltages Vg1, Vg2, and Vg3 to 0 V.
5.) Turn off supply voltages

ESD Sensitive Product

Important Information

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